ABSTRACT OF THE DISCLOSURE

The invention provides a transceiver circuit for communication that enhances the operation frequency of a synchronous digital circuit up to the maximum frequency of a flip-flop and inhibits the occurrence of jitters.

A clock signal synchronized with data at f1/n Hz is converted by a multiplier so that the signal has a frequency of "n" times so as to use the clock signal for triggering a flip-flop the operation frequency of which is f1 b/s in the synchronous digital circuit. The multiplier is arranged in the vicinity of the flip-flop triggered by the clock signal of f1 Hz so as to avoid the effect of the deterioration of the operation frequency by interconnect capacitance.

The maximum operation frequency of the transceiver circuit determined based upon the operating frequency of the synchronous digital circuit can be enhanced up to the maximum operation frequency of the flip-flop. As a margin can be produced in designing a frequency band of a clock signal processing circuit, the reduction of power consumption, the reduction of phase noise and the extension of a control frequency range can be realized.